https://dx.doi.org/10.22161/ijaers *ISSN: 2349-6495(P) | 2456-1908(O)*

Multi Channel Multi Clock Frequency Speed rate Real Time Industrial Standard Parallel PRBS CDMA Transceiver Array ASIC SOC Card Design for Ultra High Speed Wireless Communication Products/Application Cards

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Abstract— *The Aim is for HDL Design Architecture and Implementation of Multi clock frequency synchronized real time industrial standard parallel Hi-tech PRBS CDMA Transceiver Bus Array ASIC SOC /Card for Ultra high Speed real time Industrial Communication Interface Cards/Products like Data Acquisition and Tracking of wireless Data Communication Protocol Interface Cards/SOC's like Data Serializer, De-serializer, Data Communication Protocol interface ADD on cards/Products, FPGA Cards of Different Data Transfer Baud rate. This Design Consists of multiple parallel C.D.M.A Transmitters and Receiver ASIC I.P Cores , Data Transmission and Reception done by Different Clock Frequencies operated at Mega/Giga / Tera/ Peta/Exa/Zetta/Yotta/Xona/Weka Clock Frequencies. Data Transmission Speed In terms Mega/Giga/Tera/Peta/Exa/Zetta/Yotta/Xona/Weka Bytes/Frames/Super Frames etc. and also Data transmitter and receiver consists of base band signal and Carrier signal generators, Channel Encoder, Decoder, Modulator and Demodulator generates modulation and Demodulation signal by spreading and dispreading through different communication frequency spread Spectrum techniques DSSS Communication, FH , Chaos for high Bandwidth , the design done through parallel distributed computing technique, data transmission and reception done parallel for various data interface cards of different data transfer speed. In this design transmission and reception done by different PRBS Data Pattern Sequences like $2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1, $2e^{48}$-1, $2e^{52}$-1, $2e^{63}$-1 etc. H.D.L FPGA Industrial Software Design Flow Process Implementation Done by either Xilinx/Altera. Programming Done by Verilog /VHDL Software and Simulation, Synthesis, ASIC Floor planning and Placement and routing , Reconfiguration and Debugging Done Xilinx ISE 9.2i/10.1i EDA Software and Xilinx /Altera FPGA Development Board/Kit.*

Keywords— H.D.L – Hardware Description Language, P.R.B.S – Pseudo Random Binary Sequence, C.D.M.A – Code Division Multiple Access, A.S.I.C – Application Specific Integrated Circuit, S.O.C- System on Chip.

I. INTRODUCTION

In Modern Hi-tech Communication Engineering and Technology , CDMA is one of the most popular real time communication system of various Data Communication products and applications and protocols, here I am using different spread Spectrum techniques for modulation and demodulation of base band signal data at a very low frequency (50 Hz) mixed with very high frequency carrier signal (600 MHz) by spreading and de-spreading the codes using Different Spread Spectrum Communication techniques , these are Direct Sequence Spread Spectrum, Frequency Hopping, Chaos Spread Spectrum communication techniques. These Frequency Spectrums are Very High Bandwidths to cover large area networks/stations. Now Compared to other multiple access techniques Dire (like FDMA,TDMA, OFDMA etc) CDMA is very popular , this is mainly used for multiple access for multiple users at a time by spreading and de spreading of codes at cell towers /stations with high bandwidth spectrum. It saves more time for transmission and reception of data of multiple hundreds of users, Also this is very suit for high data communication and computing. CDMA Is heart of Mobile communication systems and internet communication computing stations/systems. CDMA and CDMA Array and Data Interface Cards/Boards/SOC's

are used in real time IT software MNC's and other Semiconductor and Network industries and R&D Sectors. This multi channel multi frequency parallel CDMA Transceiver ASIC SOC Consists of multiple CDMA transmitters and receivers designed parallel by purely synchronized and operated with a clock frequency of Mega/Giga/Tera/Peta/Exa/Zetta / Yotta/Xona/Weka/Vendica Hertz rate. Data transfer speed in terms of Mega/ Giga/ Tera/Peta/Exa/Zetta/Yotta/Xona/Weka/Vendica bytes /frames. Also this is very suit for HiFI smart Consumer wireless Communication products /applications like mobile phones, tablets , iphones, Note book computing system applications. Also this product is very useful for high video Data Communications like graphic images , video frame window cards ,graphic pictures and medical image diagnostics communications.

This Parallel CDMA Transmission and reception done by using different PRBS Tapped Sequence Patterns- $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{18}$-1, $2e^{23}$-1, $2e^{31}$-1 etc transmission and reception done parallel at a time for multiple user communications. Various Industrial CDMA PCB Cards/Boards Developed but compared to these this CDMA Parallel Array Transceiver ASIC SOC is so simple, flexible data transmission and reception, reducing the time delay , and improvement of performance and speed, and so reliable, at a time data transmission and reception done parallel at a time by interfacing this card for multiple data communication protocols of different baud rates and speed. This is very suit for internet and cloud computing products. This SOC has large data transmission and reception done in terms of frames/super frames/ super Verilog word frames/packets of data transmission and reception for parallel distributed data computing applications. This is very suit for large wide area network users over MNC building offices/large centers/cities/countries. Also this is very suit for all wireless consumer software design products like mobile phone cards, tablets, note book computers WiFI,LiFI Phones, LTE ASIC Phones, internet super computers etc. and space, aerospace, satellite communications ,avionics, automotive, industrial robotics automation industry EDA Cards as per Industry Standard Procedures like ITU,DO,CCITT,CENELEC,ISO etc . this parallel CDMA Array ASIC SOC Core operated at multiple clock frequencies by synchronized with tera hertz, peta, exa, zetta, Yotta, xona, weka, Vendica hertz clock frequency baud rates and data speed in terms of bytes , frames, super frames, very long word super frames, super very long word frames for very high long distance communications by synchronization of byte,frame, super frame clocks of above same frequencies. This process is simply parallel distributed computing technique of data transmission and reception.

A. Spread Spectrum Communication

- Important encoding method for wireless communications
- analog & digital data with analog signal
- spreads data over wide bandwidth
- makes jamming and interception harder
- two approaches, both in use:
  - Frequency Hopping
  - Direct Sequence
- Input is fed into a channel encoder
  - Produces analog signal with narrow bandwidth
- Signal is further modulated using sequence of digits
  - Spreading code or spreading sequence
  - Generated by pseudo noise, or pseudo-random number generator
- Effect of modulation is to increase bandwidth of signal to be transmitted
- On receiving end, digit sequence is used to demodulate the spread spectrum signal
- Signal is fed into a channel decoder to recover data

Spread Spectrum Advantages

- Immunity from various kinds of noise and multipath distortion
- Can be used for hiding and encrypting signals
- Several users can independently use the same higher bandwidth with very little interference
  - CDM/CDMA Mobile telephones
- generated by a deterministic algorithm
  - not actually random
  - but if algorithm good, results pass reasonable tests of randomness
- starting from an initial seed
- need to know algorithm and seed to predict sequence
- hence only receiver can decode signal

B. Direct Sequence Spread Spectrum

- Each bit in original signal is represented by multiple bits in the transmitted signal
- Spreading code spreads signal across a wider frequency band
  - Spread is in direct proportion to number of bits used

One technique combines digital information stream with the spreading code bit stream using exclusive-OR

C. Spread Spectrum Communication Techniques

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CDMA is a multiplexing technique used with spread spectrum

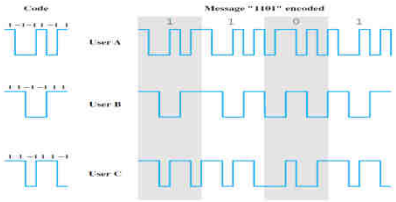
Basic Principles of CDMA

D = rate of data signal

Break each bit into *k chips*

Chips are a user-specific fixed pattern

Chip data rate of new channel = *kD*



CDMA Examples

User's codes

User A	1	−1	−1	1	−1	1
User B	1	1	−1	−1	1	1
User C	1	1	−1	1	1	−1

Transmission from A

Transmit (data bit = 1)	1	−1	−1	1	−1	1	
Receiver codeword	1	−1	−1	1	−1	1	
Multiplication	1	1	1	1	1	1	= 6

Transmit (data bit = 0)	−1	1	1	−1	1	−1	
Receiver codeword	1	−1	−1	1	−1	1	
Multiplication	−1	−1	−1	−1	−1	−1	= −6

Transmission from B, receiver attempts to recover A's transmission

Transmit (data bit = 1)	1	1	−1	−1	1	1	
Receiver codeword	1	−1	−1	1	−1	1	
Multiplication	1	−1	1	−1	−1	1	= 0

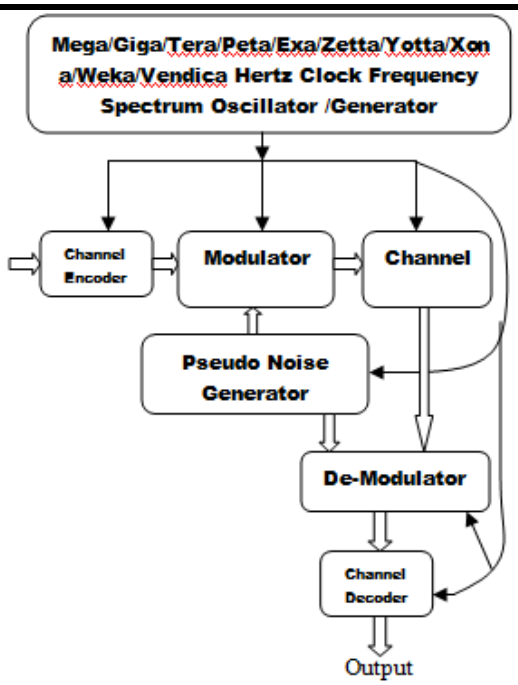
Transmission from B and C, receiver attempts to recover B's transmission

B (data bit = 1)	1	1	−1	−1	1	1	
C (data bit = 1)	1	1	−1	1	1	−1	
Combined signal	2	2	−2	0	2	0	
Receiver codeword	1	1	−1	−1	1	1	
Multiplication	2	2	2	0	2	0	= 8

Transmission from C, receiver attempts to recover B's Transmission

Transmit (data bit = 1)	1	1	−1	1	1	−1	
Receiver codeword	1	1	−1	−1	1	1	
Multiplication	1	1	1	−1	1	−1	= 2

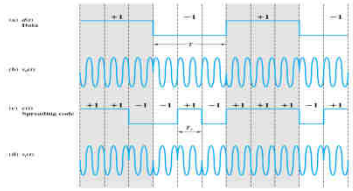
D. Multi Clock Frequency Spectrum Direct Sequence Spread Spectrum C.D.M.A Communication System Architecture



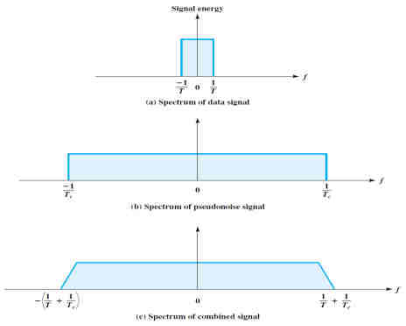
Description: The Direct Sequence Spread Spectrum C.D.M.A Communication Architecture consists of C.D.M.A Transmitter and C.D.M.A Receiver and Checker Blocks. The Transmitter Side Consists of Channel Encoder, Very High Frequency Pseudo Noise Code Carrier Frequency Generator and Modulator, whereas on receiver side consists of Demodulator , Very High Frequency Pseudo Noise Code Carrier Frequency Generator , Channel Decoder. In between Transmitter and Receiver there is a wireless communication channel path. All these blocks are operated at a ultra high frequency spectrum in terms of Mega, Giga, Tera, Peta,Exa,Zetta,Yotta,Xona,Weka,Vendica Hertz Clock Frequencies. All these above blocks are purely synchronized with these clock frequencies. This A.S.I.C S.O.C I.P Core is mainly fit and suited for future generation like 6th sense smart Digital wireless computing and communication, consumer electronic products and applications like Iphone pads, mobile phones, Video phones, cellular phones to get good voice quality for very high long distance communications etc. The operation of spread spectrum is base band signal generated with very low frequency in terms of multiple hertz and is encoded the signal and mixed with ultra high frequency Pseudo Noise Carrier Frequency Code Generator , this carrier wave modulates the very low frequency base band signal generates modulated digital signal by using different phase shift keying techniques (BPSK,PSK,QPSK etc), the modulated digital signal is propagates through wireless communication channel , and receives the signal to the receiver , on the receiver side, demodulate the received

signal is demodulated by using the Same Very High Frequency Pseudo Noise Code Frequency Generator and decode the digital signal using Channel Decoder and recovered the signal to get original base band signal (whatever feeded the signal on transmitter side) . and also can observe the clock synchronized wave forms in the below figures. This type CDMA Array Systems are Designed Parallel for transmission and reception of digital baseband signal with the help of Carrier array of Pseudo Noise Code Digital Carrier Frequency Generators of Different tapped pattern sequences $2e^{7}$-1, $2e^{10}$-1,$2e^{15}$-1, $2e^{18}$-1, $2e^{23}$-1, $2e^{31}$-1 format etc., over very wider bandwidth . the difference between old system and new system is in old system only single spread spectrum CDMA Communication systems used, but here array of Spread Spectrum CDMA systems used for parallel communication processing and controlling for various applications and products. Here I am using parallel distributed computing technique to process and control the Digital Communication signal. The speed of data signal is estimated in terms baud rate operated at above all clock frequencies. And the data transmission and reception speed in terms of mega,giga,tera,peta,exa,zetta,Yotta,xona,weka bytes and frames, super frames, very long word frames, super very long word super frames, internet data packets by purely synchronization with byte clock, frame clock, super frame clock etc.

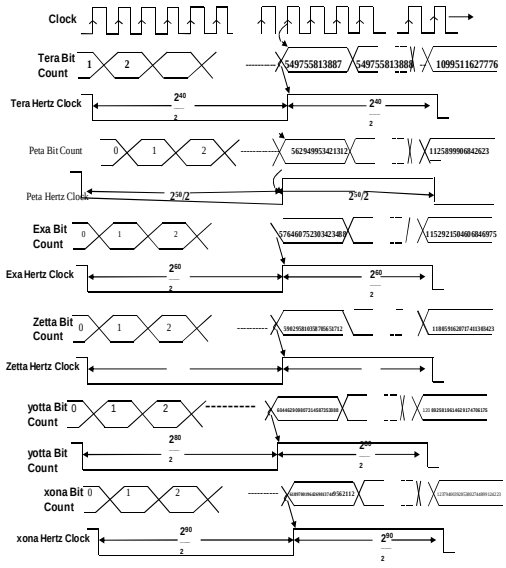
Direct Sequence Spread Spectrum using B.P.S.K
Direct Sequence Spread Spectrum Using B.P.S.K

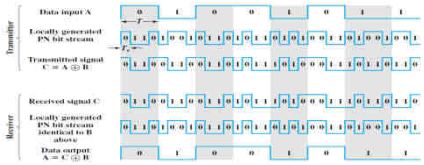


Direct Sequence Spread Spectrum Performance Consideration



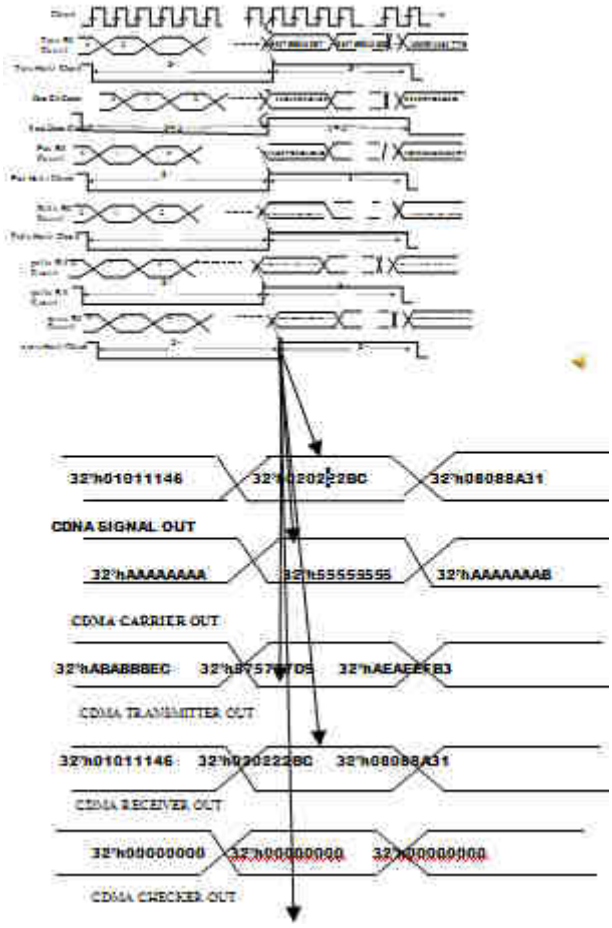
Clock Synchronization Direct Sequence Spread Spectrum Wave Form Architecture





II. Clock Synchronization Wave Form Diagrams

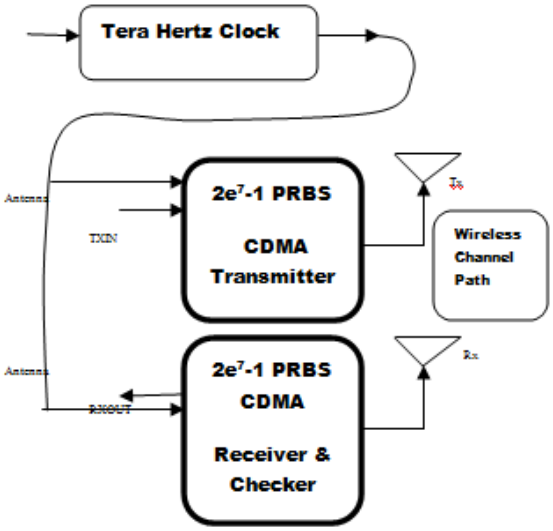
A. PRBS CDMA SOC Transceiver Design



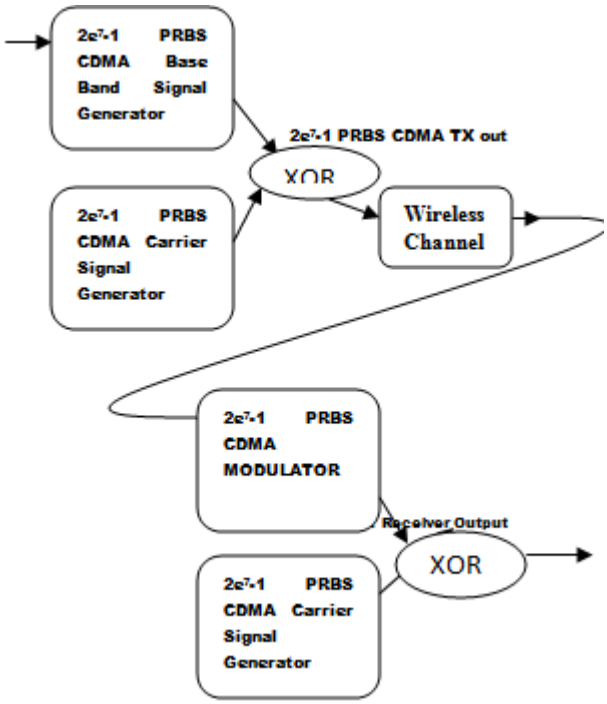
III. DESIGN ARCHITECTURE- PARALLEL PRBS CDMA

Array Transceiver ASIC S.O.C R.T.L Block

A. A.2e^7-1 PRBS CDMA Transceiver SOC Architecture

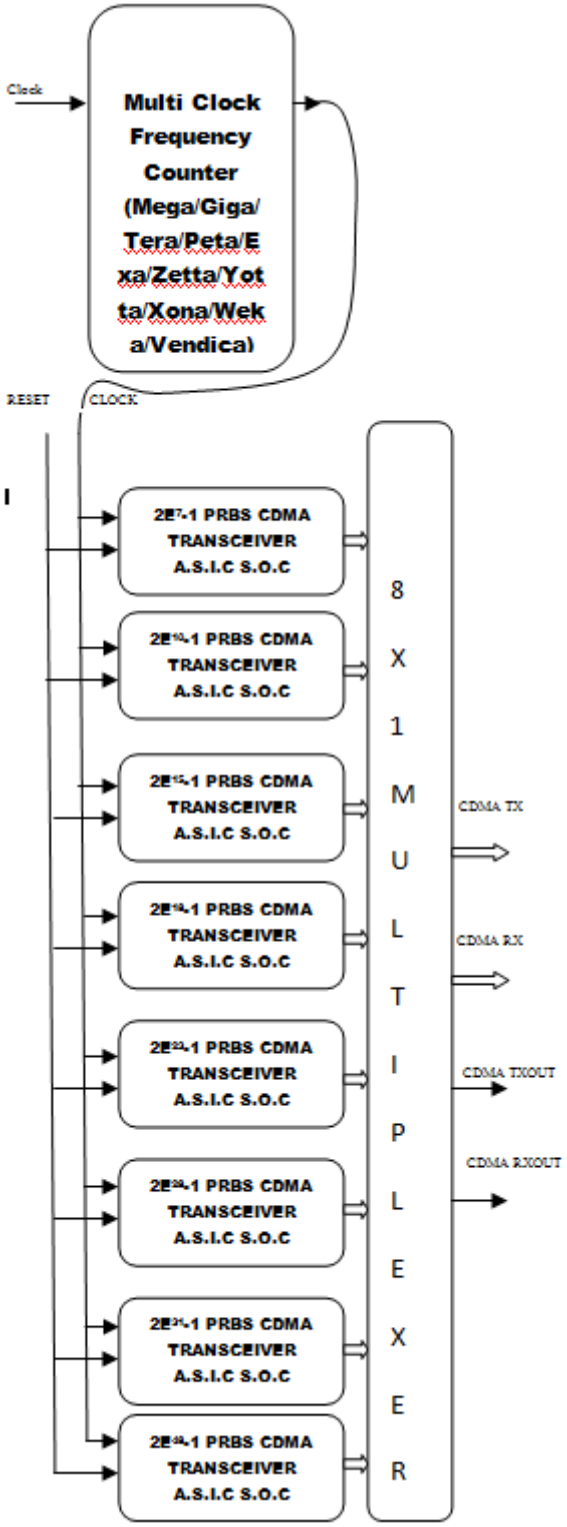


B. 2e^7-1 PRBS CDMA Transmitter

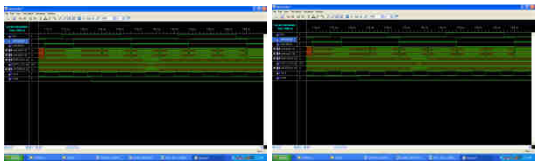


Similarly for 2e10-1, 2e15-1, 2e18-1, 2e23-1, 2e31-1 PRBS CDMA Tapped Sequence Patterns

C. Internal Functional Design Architecture

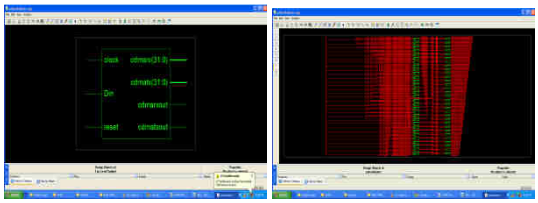


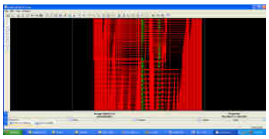
IV. SSIMULATION WAVE FORM RESULTS



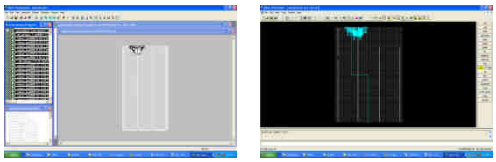
5. FPGA DESIGN FLOW REPORTS

R.T.L BLOCK **RTL Schematic**

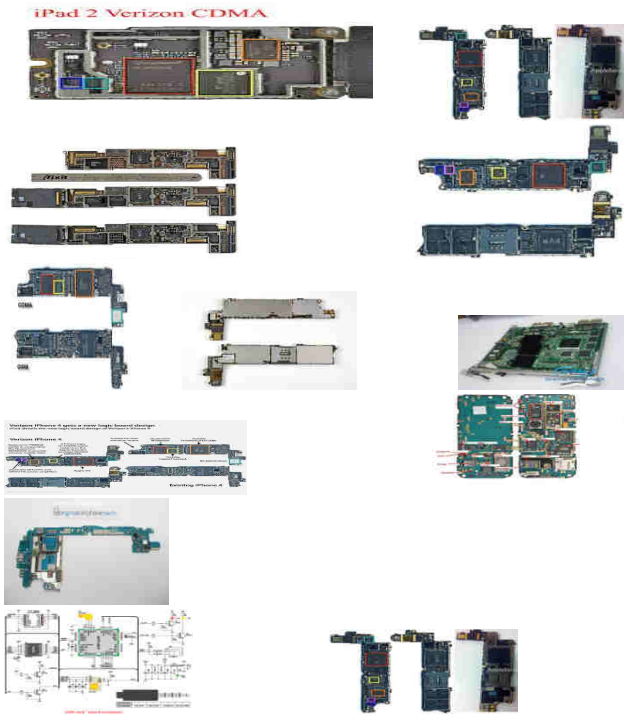




FPGA PLACED DESIGN FPGA ROUTED DESIGN



6.CDMA PCB Cards



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